Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A magnetic random access memory (MRAM) cell, comprising:

an MRAM cell stack located over a substrate and including a pinned layer, a tunneling barrier layer, and a free layer, the tunneling barrier layer interposing the pinned layer and the free layer; and

first and second write lines spanning at least one side of the MRAM cell stack and defining a projected region of intersection of the MRAM cell stack and the first and second write lines;

wherein the first write line extends in a first direction within the projected region of intersection; ~~and~~

wherein the second write line extends in a second direction within the projected region of intersection, wherein the first and second directions are angularly offset by an offset angle ranging between 45 and 90 degrees, exclusively; and

wherein neither of the first and second write lines is parallel to an easy axis of the MRAM cell stack within the projected region of intersection.

2. (Original) The MRAM cell of claim 1 wherein at least one of the first and second write lines includes a plurality of sections, each of the plurality of sections angularly offset from a neighboring one of the plurality of sections.

3. (Canceled).

4. (Original) The MRAM cell of claim 1 wherein one of the first and second write lines is substantially perpendicular to an easy axis of the MRAM cell stack within the projected region of intersection.

5. (Original) The MRAM cell of claim 1 wherein the offset angle is greater than about 75 degrees.

6. (Canceled).

7. (Original) The MRAM cell of claim 6 wherein at least one of a direction and magnitude of the angular offset relative to the substantially parallel orientation corresponds to a switching threshold shift.

8. (Original) The MRAM cell of claim 1 wherein at least one of the free layer and the pinned layer comprises a plurality of layers.

9. (Original) The MRAM cell of claim 1 wherein the first and second write lines span opposing sides of the MRAM cell stack

Claims 10-13 (Canceled).

14. (Currently Amended) An integrated circuit device, comprising:

a plurality of magnetic random access memory (MRAM) cells located over a substrate and each including a pinned layer, a tunneling barrier layer, and a free layer, the tunneling barrier layer interposing the pinned layer and the free layer; and

a plurality of first and second write lines each spanning at least one side of ones of the plurality of MRAM cells, thereby defining a plurality of projected regions of intersection of ones of the plurality of MRAM cells and corresponding ones of the first and second write lines;

wherein one of the plurality of first write lines extends in a first direction within a corresponding one of the plurality of projected regions of intersection;

wherein one of the plurality of second write lines extends in a second direction within the corresponding one of the plurality of projected regions of intersection; ~~and~~

wherein the first and second directions are angularly offset by an offset angle ranging between about 45 and about 90 degrees, exclusively; and

wherein at least one of the plurality of first and second write lines interconnects ones of the plurality of MRAM cells and has a zigzag-shaped profile.

15. (Canceled).

16. (Currently Amended) The integrated circuit device of claim [[15]] 14 wherein the interconnected ones of the plurality of MRAM cells are substantially aligned.

17. (Original) The integrated circuit device of claim 14 wherein the offset angle is greater than about 75 degrees.

18. (Original) The integrated circuit device of claim 14 wherein ones of the plurality of first and second write lines span opposing sides of ones of the plurality of MRAM cells.

19. (Original) The integrated circuit device of claim 14 wherein, for each of the plurality of MRAM cells, at least one of the first and second directions is angularly offset from an easy axis of a corresponding one of the plurality of MRAM cells, wherein at least one of a magnitude and direction of the angular offset corresponds to a switching threshold shift of the plurality of MRAM cells.

20. (Original) The integrated circuit device of claim 14 wherein at least one of the first and second directions is angularly offset from a substantially parallel orientation relative to an easy axis of a corresponding one of the plurality of MRAM cells.

21. (New) A magnetic random access memory (MRAM) cell, comprising:

an MRAM cell stack located over a substrate and including a pinned layer, a tunneling barrier layer, and a free layer, the tunneling barrier layer interposing the pinned layer and the free layer; and

first and second write lines spanning at least one side of the MRAM cell stack and defining a projected region of intersection of the MRAM cell stack and the first and second write lines;

wherein the first write line extends in a first direction within the projected region of intersection;

wherein the second write line extends in a second direction within the projected region of intersection, wherein the first and second directions are angularly offset by an offset angle ranging between 45 and 90 degrees, exclusively; and

wherein at least one of the first and second write lines includes a plurality of sections, each of the plurality of sections angularly offset from a neighboring one of the plurality of sections.

22. (New) The MRAM cell of claim 21 wherein one of the first and second write lines is substantially perpendicular to an easy axis of the MRAM cell stack within the projected region of intersection.

23. (New) The MRAM cell of claim 21 wherein the offset angle is greater than about 75 degrees.

24. (New) The MRAM cell of claim 21 wherein one of the first and second directions is angularly offset from a substantially parallel orientation relative to an easy axis of the MRAM cell stack.

25. (New) The MRAM cell of claim 24 wherein at least one of a direction and magnitude of the angular offset relative to the substantially parallel orientation corresponds to a switching threshold shift.

26. (New) The MRAM cell of claim 21 wherein at least one of the free layer and the pinned layer comprises a plurality of layers.

27. (New) The MRAM cell of claim 21 wherein the first and second write lines span opposing sides of the MRAM cell stack.